

WHAT IS CLAIMED IS:

1. An FM transmitter, comprising:
a phase lock loop including a charging pump;
5 an adder to add up a frequency shift to a signal of
said phase lock loop, said frequency shift corresponding
to a transmission signal; and
a controller to receive a signal regarding start and
idle of said phase lock loop, and to output a control
10 signal to control an output of said charging pump.

2. The FM transmitter according to claim 1,
wherein said FM transmitter further comprises:
a buffer amplifier to input a signal from said phase
15 lock loop and to output a signal to an antenna,
wherein said controller further receives a signal
regarding start and idle of said buffer amplifier, and
outputs a control signal to control an output of said
charging pump to switch status of said phase lock loop
20 between open and closed.

3. An FM transmitter according to claim 1,
wherein said phase lock loop further includes a phase
comparator, a loop filter, a voltage controlled
25 oscillator, and a counter,
wherein said FM transmitter further comprises to
output a signal to an antenna, and
wherein said FM transmitter further comprises a
controller to receive a start/idle signal of said phase

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lock loop, as well as a start/idle signal of said buffer amplifier and to output a control signal to hold an output of said charging pump in a high resistance state.

- 5 4. The FM transmitter according to claim 3,
 wherein said controller comprises:

 a delay circuit to delay a start/idle signal of said buffer amplifier; and

- a flip-flop circuit to receive an output of said
10 delay circuit at one input terminal and a start/idle signal of said phase lock loop at the other input terminal, said flip-flop circuit being set by said start/idle signal of said phase lock loop and reset by said output of said delay circuit, and

- 15 wherein said phase lock loop is controlled so as to be held in closed loop control between a start-up timing of said phase lock loop and a timing delayed by a certain time from said start-up of said buffer amplifier and held in open loop control in other periods.

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5. The FM transmitter according to claim 3,

- wherein said controller comprises a preamble detector to detect a preamble signal included in said transmission signal and a flip-flop circuit to be set by said
25 start/idle signal of said phase lock loop and reset by said output of said preamble detector, and

 wherein said phase lock loop is controlled so as to be held in closed loop control between a start-up timing of said phase lock loop and a transmission timing of said

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preamble signal, and held in open loop control in other periods.

5 6. The FM transmitter according to claim 3,
 wherein said charging pump is provided with a logical
circuit to suppress a frequency control signal output from
said phase comparator according to a control signal output
from said controller.

10 7. The FM transmitter according to claim 4,
 wherein said charging pump is provided with a logical
circuit to suppress a frequency control signal output from
said phase comparator according to a control signal output
from said controller.

15 8. The FM transmitter according to claim 5,
 wherein said charging pump is provided with a logical
circuit to suppress a frequency control signal output from
said phase comparator according to a control signal output
20 from said controller.

 9. The FM transmitter according to claim 3,
 wherein said charging pump is provided with a switch
to reset a bias current to zero according to a control
25 signal output from said controller.

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10. The FM transmitter according to claim 4,
wherein said charging pump is provided with a switch
to reset a bias current to zero according to a control
signal output from said controller.

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11. The FM transmitter according to claim 5,
wherein said charging pump is provided with a switch
to reset a bias current to zero according to a control
signal output from said controller.

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12. The FM transmitter according to claim 3,
wherein said controller comprises:

an offset detector to detect an offset of the number
of "H" or "L" generated transmission signals, said offset
detector detecting whether an absolute integration value
that denotes said offset of the number of generated "H" or
"L" transmission signals, obtained by integrating said
transmission signals, exceeds a predetermined threshold;
and

a flip-flop circuit to be set by said start/idle
signal of said phase lock loop and reset by said output of
said offset detector, and

wherein said phase lock loop is controlled so as to
be held in closed loop control between a phase lock loop
start-up timing and a timing of detection of said
predetermined threshold exceeded by said offset of the
number of "H" or "L" generated transmission signals by
said offset detector and to be held in open loop control
in other periods.

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13. A transmitter to transmit a signal with FM modulation, wherein the transmitter receives a start/idle signal of a phase lock loop circuit and a start/idle signal of a buffer amplifier, and outputs a control signal
5 to hold an output of a charging pump at a first level of resistance at which a bias current is substantially zero, and

wherein said phase lock loop circuit is moved into open loop control when the output of the charge pump is
10 held at the first level of resistance.

14. The transmitter for FM transmission according to claim 13;

wherein said signal to be transmitted has a preamble,
15 and said phase lock loop circuit is controlled for the loop to be closed or opened based on said preamble.

15. The transmitter for FM transmission according to claim 13,

20 wherein said transmitter includes a controller comprising:

a delay circuit to delay a start/idle signal of said buffer amplifier; and

a flip-flop circuit to receive an output of said
25 delay circuit at one input terminal and a start/idle signal of said phase lock loop at the other input terminal, said flip-flop circuit being set by said start/idle signal of said phase lock loop and reset by said output of said delay circuit, and

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wherein said phase lock loop is controlled so as to be held in closed loop control between a start-up timing of said phase lock loop and a timing delayed by a certain time from said start-up of said buffer amplifier, and held
5 in open loop control in other periods.

16. The transmitter for FM transmission according to claim 13,

wherein said transmitter includes a controller
10 comprising a preamble detector to detect a preamble signal included in said transmission signal and a flip-flop circuit to be set by said start/idle signal of said phase lock loop and reset by said output of said preamble detector, and

15 wherein said phase lock loop is controlled so as to be held in closed loop control between a start-up timing of said phase lock loop and a transmission timing of said preamble signal, and held in open loop control in other periods.

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17. An FM transmitter, comprising:

a phase lock loop not including a sample-and-hold circuit; and

an adder to add up a frequency shift to a signal of
25 said phase lock loop, said frequency shift corresponding to a transmission signal,

wherein said phase lock loop is controlled to switch status of said phase lock loop between open and closed without the use of a sample-and-hold circuit.

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18. The FM transmitter according to claim 17,
wherein said phase lock loop includes a charging
pump, and

wherein said FM transmitter includes a controller to
5 receive a signal regarding start and idle of said phase
lock loop, and to output a control signal to control an
output of said charging pump.

19. The FM transmitter according to claim 17,
10 wherein said FM transmitter includes a buffer
amplifier to input a signal from said phase lock loop and
to output a signal to an antenna,

wherein said buffer amplifier is provided to receive
a signal regarding start and idle of said buffer amplifier
15 through from another path than the path from said phase
lock loop.

20. The FM transmitter according to claim 17,
wherein said phase lock loop includes a charging
20 pump, and

wherein said FM transmitter further comprises:
a buffer amplifier to input a signal from said phase
lock loop and to output a signal to an antenna; and
a controller to receive a signal regarding start and idle
25 of said phase lock loop and a signal regarding start and
idle of said buffer amplifier, and to output a control
signal to control an output of said charging pump to
switch status of said phase lock loop between open and
closed.

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